

SWARUP BHUNIA, PHD

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PROFESSIONAL PREPARATION

Purdue University Electrical and Comp. Engg. Ph. D. 2005
Thesis: Power and Yield-Aware Design and Test of Nano-Scale CMOS Circuits.

Indian Institute of Technology, Kharagpur Computer Science M. S. 1997
Thesis: Design and Simulation of an ASIC for Fractal Image Compression.

Jadavpur University, Kolkata Computer Science B. E. 1995

APPOINTMENTS

7/2011-Present	Associate Professor	Electrical Engineering and Computer Science, CWRU
8/2005-6/2011	Assistant Professor	Electrical Engineering and Computer Science, CWRU
5/2003-8/2003	Summer Intern	Intel Corporation
5/2002-8/2002	Summer Intern	Intel Corporation
9/1997-7/2000	Senior Engineer	Interra Systems

RESEARCH INTERESTS

- Bioimplantable electronics
- Hardware security
- Adaptive nanoscale computing
- Low-power and robust system design
- Computing at extreme

ACHIEVEMENTS / AWARDS

- IBM Faculty Award, July 2013
- Appointment for T. and A. Schroeder Professorship in Computer Science and Engineering, May 2013
- Excellence in Teaching award, EECS, Case Western Reserve University, 2012
- Best paper award, 25th International Conference on VLSI Design, 2012
- National Science Foundation (NSF) career development (CAREER) award, 2011
- Mike Mesarovic award for extraordinary impact, in the department of EECS, Case Western Reserve U., 2011
- Nomination for Case School of Engineering Research Achievement Award, 2011
- Nomination for John S. Diekhoff Graduate Student Mentoring Award, Case Western Reserve U., 2010

- Best paper candidate, *IEEE Hardware Oriented Security and Trust Symposium (HOST)*, 2010
- Semiconductor Research Corporation (SRC) Inventor Recognition Award, 2009
- Outstanding Teacher Award, EECS, Case Western Reserve University, 2008
- Best paper nomination in *Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2006
- Semiconductor Research Corporation (SRC) Technical Excellence award, 2005
- E.J. McCluskey Best Doctoral Thesis Award by *Test Technology Technical Council (TTTC)* of IEEE Computer Society, 2005, 3rd place winner.
- Best paper award in *International Conference on Computer Design (ICCD)*, 2004
- Best paper award in *Latin American Test Workshop (LATW)*, 2003.

PROPOSAL ACTIVITY

Active Grants:

1. 07/01/10- 06/30/13 Source: NSF Location: CWRU

Title: Collaborative Research: Reconfigurable Computing Using 2D Nanoscale Memory for Multimedia Signal Processing (with Georgia Tech)

Calendar: 00.00 Academic: 0 Summer: 0.50

Swarup Bhunia (PI) 100%

2. 09/09/10-09/08/13 Source: NSF Location: CWRU

Title: SHF: Medium: Collaborative Research: System Level Self Correction Using On-Chip Micro Sensor Network and Autonomous Feedback Control (with Purdue University)

Calendar: 00.00 Academic: 0 Summer: 1.00

Swarup Bhunia (PI) 100%

3. 04/01/11 – 03/31/14 Source: DARPA Location: CWRU

Title: Techniques for Validation and Integrity of Soft IP Cores

Calendar: 00.00 Academic: 0.45 Summer: 1

Christos Papachristou (PI) 55%, Steve Clay, Rockwell Automation (Co-PI) 25%, **Swarup Bhunia (Co-PI) 20%**

4. 08/01/08 – 08/31/11 Source: NSF Location: CWRU

Title: Batch-Fabricated Nanochannel Devices for Direct Electrical Probing of Biomolecules

Calendar: 00.00 Academic: 0 Summer: 0.25

Carlos Mastrangelo, U. Of Utah (PI) 65%, **Swarup Bhunia (Co-PI) 35%**

5. 06/01/08-05/31/11 Source: Intel Corporation Location: CWRU

Title: Fine-Grain Power Management & Monitoring Circuits

Calendar: 00.00 Academic: 0.45 Summer: 0.50

Swarup Bhunia (PI) 100%

6. 02/01/11-01/31/12 Source: Intel Corporation Location: CWRU

Title: Width-Aware Dynamic Supply Gating for Low Power Datapath & Memory

Calendar: 00.00 Academic: 0 Summer: 1.00

Swarup Bhunia (PI) 100%

7. 07/01/11- 06/30/16 Source: NSF Location: CWRU

Title: CAREER: An Integrative and Scalable Approach to Embedded Hardware Protection

Calendar: 00.00 Academic: 0 Summer: 0.25

Swarup Bhunia (PI) 100%

8. 09/01/11- 08/31/14 Source: NSF Location: CWRU

Title: SHF:Small: Device-Circuit-Architecture Co-Design for Reconfigurable Computing at the Extreme
Calendar: 00.00 Academic: 0 Summer: 0.125

Swarup Bhunia (PI) 50%, Mehran Mehregany (Co-PI) 20%, Philip Feng (Co-PI) 30%

9. 08/01/11 – 07/31/12 Source: DARPA Location: CWRU

Title: Electromechanical Computing at High Temperature Using Poly-SiC NEMS

Calendar: 00.00 Academic: 0.45 Summer: 1.00

Mehran Mehregany (PI), 50%, **Swarup Bhunia (Co-PI) 35%**, Philip Feng (Co-PI) 15%

10. 04/01/12- 03/31/16 Source: VA Location: CWRU

Title: Wireless Implantable Pressure Monitor for Improved Neuromodulation (with Cleveland Clinic Foundation)

Calendar: 00.00 Academic: 0 Summer: 0.5

Margot Damaser (PI), Wen Co (Co-I), Steve Garverick (Co-I), Ken Gustavson (Co_I), **Swarup Bhunia (Co-I) 15%**

Completed Grants:

1. 05/01/2008 – 04/31/2009 Source: DARPA/AFRL Location: CWRU

Title: Minimally Invasive Multi-Parameter Side-Channel Approach for Sequential Trojan Detection

Swarup Bhunia (PI) 60%, Chris Papachristou (Co-PI) 15%, Francis Wolff (Co-PI): 10%, Kaushik Roy, Purdue (Co-PI) 15%

Calendar: 00.00 Academic: 10% Summer: 1.50

2. April, 2007 – April, 2008 Source: DARPA Location: CWRU

Title: Standby Leakage Reduction and Data Retention Using Hybridization with SiC NEMS Switches

Mehran Mehregany (PI) 80%, **Swarup Bhunia (Co-PI) 20%**

Calendar: 00.00 Academic: 5% Summer: 1.00

3. 01/01/09-12/31/10 Source: DARPA Location: CWRU

Title: High-Temperature Logic Using Poly-SiC NEMS

Calendar: 00.00 Academic: 0.90 Summer: 1.00

Mehran Mehregany (PI) 75%, **Swarup Bhunia (Co-PI) 25%**

Equipment Grants:

1. 04/06/07 Altera Corporation donated one FPGA Development Board + Quartus software suite

2. 05/01/08 Intel Corporation donated two high-performance desktop computers

3. 04/06/07 Xilinx Corporation donated five FPGA Development Boards + ISE software suite

PUBLICATIONS/PATENTS

[Papers marked in [blue](#) are based on individual/collaborative work of Dr. Bhunia after joining Case. Underlined authors are Case students supervised by Dr. Bhunia.]

Journal Publications:

Published/Accepted for publication

1. [Anandaroop Ghosh](#), [Somnath Paul](#), Jongsun Park, and **Swarup Bhunia**, “Improving Energy Efficiency in FPGA through Judicious Mapping of Computation to Embedded Memory Blocks”, to appear in *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*.
2. [Seetharam Narasimhan](#), [Dongdong Du](#), [Rajat Subhra Chakraborty](#), [Somnath Paul](#), Francis Wolff, Christos Papachristou, Kaushik Roy, and **Swarup Bhunia**, “Hardware Trojan Detection by Multiple-Parameter Side-

- Channel Analysis”, *IEEE Transactions on Computers*.
3. [Seetharam Narasimhan](#), Wen Yueh, [Xinmu Wang](#), Saibal Mukhopadhyay, and **Swarup Bhunia**, “Improving IC Security against Trojan Attacks through Integration of Security Monitors”, *IEEE Design & Test of Computers (D&T) Special Issue on Smart Silicon*.
 4. **Swarup Bhunia**, Miron Abramovici, Dakshi Agarwal, Paul Bradley, Michael S. Hsiao, Jim Plusquellic, and Mohammad Tehranipoor, “Protection against Hardware Trojan Attacks: Towards a Comprehensive Solution”, *IEEE Design & Test of Computers*, 2012.
 5. [Seetharam Narasimhan](#), [Keerthi Kunaparaju](#), **Swarup Bhunia**, “Healing of DSP Circuits under Power Bound Using Post-Silicon Operand Bitwidth Truncation”, *IEEE Transactions on CAS I (TCAS-I)*.
 6. [Rajat Subhra Chakraborty](#) and **Swarup Bhunia**, “Security Against Hardware Trojan Attacks Using Key-based Design Obfuscation”, *Journal of Electronic Testing: Theory and Applications (JETTA)*, Vol. 27, Issue 6, Nov 2011.
 7. [Somnath Paul](#), Subho Chatterjee, Saibal Mukhopadhyay and **Swarup Bhunia**, “Energy-Efficient Reconfigurable Computing Using a Circuit-Architecture-Software Co-Design Approach”, *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, 2011. [Special issue on Advances in Design of Energy-Efficient Circuits and Systems]
 8. [Seetharam Narasimhan](#), [Rajat Subhra Chakraborty](#), and **Swarup Bhunia**, “Hardware IP Protection during Evaluation Using Embedded Sequential Trojan”, *IEEE Design & Test of Computers*, 2011.
 9. [Somnath Paul](#), Saibal Mukhopadhyay and **Swarup Bhunia**, “A Variation-Aware Preferential Design Approach for Memory Based Reconfigurable Computing”, *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, 2011.
 10. [Somnath Paul](#), Fang Cai, Xinmiao Zhang, and **Swarup Bhunia**, “Reliability-Driven ECC Allocation for Multiple Bit Error Resilience in Processor Cache”, *IEEE Transactions on Computers (TCOMP) Special Issue on Dependable Computer Architecture*, Feb 2011.
 11. [Seetharam Narasimhan](#), Hillel Chiel and **Swarup Bhunia**, “Ultra Low-Power and Robust Digital Signal Processing Hardware for Implantable Neural Interface Microsystems”, *IEEE Transactions on Biomedical Circuits and Systems (TBioCAS)*, April 2011.
 12. Te-Hao Lee, **Swarup Bhunia**, and Mehran Mehregany, “Electromechanical Computing at 500 °C with Silicon Carbide”, *Science*, Sept 10, 2010, vol. 329, no. 5997, pp. 1316-1318.
 13. [Somnath Paul](#) and **Swarup Bhunia**, “Dynamic Transfer of Computation to Processor Cache for Yield and Reliability Improvement”, *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, 2010.
 14. [Somnath Paul](#), Saibal Mukhopadhyay and **Swarup Bhunia**, "Circuit and Architecture Co-design Approach for Hybrid CMOS-STTRAM non-volatile FPGA", *IEEE Transactions on Nanotechnology (TNANO)*, 2010.
 15. [Somnath Paul](#) and **Swarup Bhunia**, "A Scalable Memory-Based Reconfigurable Computing Framework for Nanoscale Crossbar", *IEEE Transactions on Nanotechnology (TNANO)*, 2010.
 16. [Rajat Subhra Chakraborty](#) and **Swarup Bhunia**, “A Study of Asynchronous Design Methodology for Robust CMOS-Nano Hybrid System Design”, *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, vol. 5, no. 3, pp. 12:1-12:22, Aug 2009.
 17. [Somnath Paul](#), Hamid Mahmoodi and **Swarup Bhunia**, "Low-Overhead F_{max} Calibration at Multiple Operating Points Using Delay Sensitivity Based Path Selection," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 15, no. 2, pp. 19.1:19.34, Feb 2010.
 18. [Rajat Subhra Chakraborty](#) and **Swarup Bhunia**, "HARPOON: An Obfuscation based SoC Design Methodology for Hardware Protection," *IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 28, no. 10, pp. 1493-1502, 2009.
 19. [Rajat Subhra Chakraborty](#), [Somnath Paul](#), [Yu Zhou](#), and **Swarup Bhunia**, "Low-Power Hybrid CMOS-NEMS FPGA: Circuit Level Analysis and Defect-Aware Mapping," *IET Computers and Digital Techniques (IET-CDT)*, vol. 3, no. 6, pp. 609-624, 2009.
 20. Patrick Ndai, Nauman Rafique, Mithuna Thottethodi, Swaroop Ghosh, **Swarup Bhunia**, and Kaushik Roy, "Trifecta: A Non-Speculative Scheme to Exploit Common, Data-Dependent Subcritical Paths," *IEEE Trans. on Very Large Scale Integration Systems (TVLSI)*, vol. 18, no. 1, pp. 53-65, 2009.
 21. Patrick Ndai, **Swarup Bhunia**, Amit Agarwal, and Kaushik Roy, “Within-Die Variation-Aware Scheduling in Superscalar Processors for Improved Throughput”, *IEEE Transactions on Computers*, vol. 57, no. 7, pp. 940-951, 2008.

22. **Swarup Bhunia**, Hamid Mahmoodi, Arijit Raychowdhury, and Kaushik Roy, "Arbitrary Two-Pattern Delay Testing Using A Low-Overhead Supply Gating Technique", *Journal of Electronic Testing: Theory and Applications (JETTA)*, vol. 24, no. 6, pp. 577-590, 2008.
23. Animesh Datta, **Swarup Bhunia**, Jung Hwan Choi, Saibal Mukhopadhyay, and Kaushik Roy "Profit Aware Circuit Design under Process Variations Considering Speed Binning", *IEEE Transactions on Very Large Scale Integration Systems*, vol. 16, no. 7, pp. 806-815, 2008.
24. Rajat Subhra Chakraborty, Seetharam Narasimhan, and **Swarup Bhunia**, "Hybridization of CMOS with CNT-Based Nano Electromechanical Switch for Low Leakage and Robust Circuit Design Using Nanoscaled CMOS Devices", *IEEE Transactions on Circuits and Systems I (TCAS I)*, vol. 54, no. 11, pp. 2480-2488, 2007.
25. Swaroop Ghosh, **Swarup Bhunia**, and Kaushik Roy, "Low-Power and Testable Circuit Synthesis Using Shannon Decomposition Based Structural Transformation", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 12, no. 4, pp. 47:1-47:6, 2007.
26. Amit Agarwal, Kunhyuk Kang, **Swarup Bhunia**, James Gallagher, and Kaushik Roy, "Device-Aware Yield-Centric Dual-Vt Design under Parameter Variations in Nano-Scale Technologies", *IEEE Transactions on Very Large Scale Integration Systems*, vol. 15, no. 6, pp. 660-671, 2007.
27. Swaroop Ghosh, **Swarup Bhunia**, and Kaushik Roy, "CRISTA: A New Paradigm for Low-power, Variation-Tolerant and Adaptive Circuit Synthesis Using Critical Path Isolation", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, vol. 26, no. 11, pp. 1947-1956, 2007 [**Top 10 downloaded papers in Nov 2007**].
28. Nilanjan Banerjee, Arijit Raychowdhury, Kaushik Roy, **Swarup Bhunia**, and Hamid Mahmoodi, "Novel Low-Overhead Operand Isolation Techniques for Low-Power Datapath Synthesis", *IEEE Transactions on Very Large Scale Integration Systems*, vol. 14, no. 9, pp. 1034-1039, 2006.
29. Swaroop Ghosh, **Swarup Bhunia**, Arijit Raychowdhury, and Kaushik Roy, "A Novel Delay Fault Testing Methodology Using Low Overhead Built-In Delay Sensor", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, vol. 25, no. 12, pp. 2934-2943, 2006.
30. Animesh Datta, **Swarup Bhunia**, Saibal Mukhopadhyay, and Kaushik Roy, "Delay Modeling and Statistical Design of Pipelined Circuit under Process Variation", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 25, no. 11, pp. 2427-2436, 2006.
31. Saibal Mukhopadhyay, **Swarup Bhunia**, and Kaushik Roy, "Modeling and Analysis of Loading Effect on Leakage of Nanoscaled Bulk-CMOS Logic Circuits", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 25, no. 8, pp. 1486-1495, 2006.
32. Arijit Raychowdhury, Bipul Paul, **Swarup Bhunia**, and Kaushik Roy, "Computing with Sub-threshold Leakage: Device/Circuit/Architecture Co-design for Ultralow-power Subthreshold Operation", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 13, no. 11, pp. 1213-1224, 2005.
33. Qikai Chen, Hamid Mahmoodi, **Swarup Bhunia**, and Kaushik Roy, "Efficient testing of SRAM with optimized March sequences and a Novel DFT Technique for emerging failures due to process variations", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 13, no. 11, pp. 1286-1295, 2005.
34. **Swarup Bhunia** and Kaushik Roy, "A novel wavelet transform-based transient current analysis for fault detection and localization", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 13, no. 4, pp. 503-507, 2005.
35. **Swarup Bhunia**, Animesh Datta, Nilanjan Banerjee, and Kaushik Roy, "GAARP: A Power-Aware GALS Architecture for Real-Time Algorithm-Specific Tasks", *IEEE Transactions on Computers (TCOMP)*, vol. 54, no. 6, pp. 752-766, 2005.
36. **Swarup Bhunia**, Hamid Mahmoodi, Saibal Mukhopadhyay, Debjyoti Ghosh, and Kaushik Roy, "Low-Power Scan Design Using First Level Supply Gating", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 13, no. 3, pp. 384-395, 2005.
37. **Swarup Bhunia**, Arijit Roychowdhury, and Kaushik Roy, "Frequency Specification Testing of Analog Filters Using Wavelet Transform of Dynamic Supply Current", *Journal of Electronic Testing: Theory and Applications (JETTA)*, vol. 21, no. 3, pp. 243-255, 2005.
38. Lih-yih Chiou, **Swarup Bhunia**, and Kaushik Roy, "Synthesis of Application-Specific Highly Efficient Multi-Mode Cores for Embedded Systems", *ACM transactions on Embedded Computing System (TECS)*, vol. 4, no. 1, pp. 168-188, 2005.

39. **Swarup Bhunia**, Arijit Raychowdhury, and Kaushik Roy, "Defect Oriented Testing of Analog Circuits Using Wavelet Analysis of Dynamic Supply Current", *Journal of Electronic Testing: Theory and Applications (JETTA)*, vol. 21, no. 2, pp. 147-159, 2005.
40. Hai Li, **Swarup Bhunia**, Yiran Chen, Kaushik Roy, and T. N. Vijaykumar, "DCG: Deterministic Clock-Gating for Low-Power Microprocessor Design", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 12, no. 3, pp. 245-254, 2004.

Editorials:

- [1] Swarup Bhunia, Leyla Nazhandali, and Dakshi Agrawal, "Guest Editors' Introduction: Trusted System with Untrusted Components: An Emerging Design Need", *IEEE Design & Test of Computers*, April 2013.
- [2] Swarup Bhunia and Darrin J. Young, "Introduction to Special Issue on Implantable Electronics", *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, Vol. 8, No. 2, pp. 7.1-7.2, June 2012.
- [3] Swarup Bhunia and Rahul Rao, "Guest Editors' Introduction: Managing Uncertainty through Postfabrication Calibration and Repair", *IEEE Design & Test of Computers*, Vol. 27, No. 6, pp. 4-5, November 2010.
- [4] Swarup Bhunia and Saibal Mukhopadhyay, "Preface" in *Low-Power Variation Tolerant Design in Nanometer Silicon*, Springer, New York, USA, 1st Edition, ISBN:1441974172, November 2010.
- [5] Swarup Bhunia, "A Special Issue on 23rd IEEE International Conference on VLSI Design, Bangalore, India, 3-7 January 2010", *Journal of Low Power Electronics (JOLPE)*, Vol. 6, No. 3, pp. 375-375, October 2010.

Conference Publications:

Invited Articles

1. Abhishek Basak, Yu Zheng, Jangwon Park, Jongsun Park, and Swarup Bhunia, "Reconfigurable ECC for Adaptive Protection of Memory", to appear in *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2013. [Invited article in special session on Self-Healing and Self-adaptive RF/Mixed-signal circuits for low-cost, high-yield and robust systems].
2. Xinmu Wang, Seetharam Narasimhan, Aswin Krishna, Tatini Mal-Sarkar, and **Swarup Bhunia**, "Sequential Hardware Trojan Attacks: Experiences from ESC 2010", *29th IEEE International Conference on Computer Design (ICCD)*, 2011. [Invited in the special session "Capture the Chip"]
3. Hadi Hajimiri, Somnath Paul, Anandaroop Ghosh, **Swarup Bhunia**, and Prabhat Mishra, "Reliability Improvement in Many-Core Architectures through Computing in Embedded Memory", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2011. [Invited article in special session on self-healing circuits in scaled technologies].
4. Srihari Rajgopal, Philip X.-L. Feng, **Swarup Bhunia** and Mehran Mehregany, "Nano Manufacturing of SiC Circuits — Nanomechanical Logic and NEMS-JFET Integration", *Technologies for Future Micro-Nano Manufacturing Workshop*, Aug 8-10, 2011. [Invited 2-page abstract]
5. Seetharam Narasimhan, Jongsun Park, and **Swarup Bhunia**, "Digital Signal Processing in Bio-implantable Systems: Design Challenges and Emerging Solutions", *The Asia Symposium on Quality Electronic Design (ASQED)*, 2010. [Invited paper in special session on bio-sensing and bio-system design].
6. Swarup Bhunia and Anand Raghunathan, "Hardware Security: Design, Test and Validation Issues", Hot topic Special Session in *IEEE VLSI Test Symposium (VTS)*, pp. 349-349, 2010. [Invited article on the special session]
7. Rajat Subhra Chakraborty, Seetharam Narasimhan, and **Swarup Bhunia**, "Hardware Trojan: Threats and Emerging Solutions", *IEEE International High Level Design Validation and Test Workshop (HLDVT)*, pp. 166-171, 2009. [Invited paper in the special session on post-silicon validation]
8. Somnath Paul and **Swarup Bhunia**, "Computing with Nanoscale Memory: Model and Architecture," *IEEE/ACM International Symposium on Nanoscale Architecture (NANOARCH)*, pp. 1-6, 2009. [Invited paper]
9. **Swarup Bhunia** and Kaushik Roy, "Low Power Design under Parameter Variations", *International*

- Symposium on Low Power Electronics and Design (ISLPED)*, 2008. [One page article on embedded tutorial]
10. **Swarup Bhunia** and Kaushik Roy, “Power Dissipation, Variations and Nanoscale CMOS Design: Test Challenges and Self-Calibration/Self-Repair Solutions”, *International Test Conference (ITC)*, pp. 1-10, 2007. [Lecture series article]
 11. **Swarup Bhunia**, Saibal Mukhopadhyay, and Kaushik Roy, “Process Variations and Process-Tolerant Design”, *International Conference on VLSI Design*, pp. 699-704, 2007.

Peer-Reviewed Articles

Published/Accepted for publication

12. Hadi Hajimiri, Prabhat Mishra, **Swarup Bhunia**, Branden Long, Yibo Li, and Rashmi Jha, “Content-aware Encoding for Improving Energy Efficiency in Resistive Random Access Memory”, *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, 2013.
13. Vaishnavi Ranganathan, Tina He, Srihari Rajgopal, Mehran Mehregany, Philip Feng, and **Swarup Bhunia**, “Robust Nanomechanical Non-Volatile Memory for Computing at Extreme”, *9th IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, 2013.
14. Yu Zheng, MaryamSadat Hashemian, and **Swarup Bhunia**, “RESP: A Robust Physical Unclonable Function Retrofitted into Embedded SRAM Array”, *Design Automation Conference (DAC)*, 2013.
15. Xinmu Wang, Wen Yueh, Debapriya Basu Roy, Yu Zheng, Seetharam Narasimhan, Saibal Mukhopadhyay, Debdeep Mukhopadhyay, and **Swarup Bhunia**, “Role of Power Grid in Side Channel Attack and Power-Grid-Aware Secure Design”, *Design Automation Conference (DAC)*, 2013.
16. Tina He, Vaishnavi Ranganathan, Rui Yang, Srihari Rajgopal, **Swarup Bhunia**, Mehran Mehregany, and Philip X.-L. Feng, “Time-Domain AC Measurement of SiC Nanoelectromechanical Switches toward High Speed Operations”, *The 17th International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers)*, 2013.
17. Yibo Li, Wenbo Chen, Ammaarah El-Amin, Rashmi Jha, **Swarup Bhunia**, and Philip X.-L. Feng, “A Reconfigurable Sensing and Computing Platform for Artificial Electronic Skins”, *MRS Spring Meeting (Symposium TT: Materials and Processes for Artificial Skin)*, April 2013.
18. Tina He, Rui Yang, Srihari Rajgopal, **Swarup Bhunia**, Mehran Mehregany, and Philip X.-L. Feng, “Dual-gate silicon carbide (SiC) lateral nanoelectromechanical switches”, *The 8th Annual IEEE International Conference on Nano/Micro Engineered and Molecular Systems (NEMS)*, 2013. **[Best Student Paper Award]**
19. Xinmu Wang, Seetharam Narasimhan, Aswin Krishna, Tatini Mal-Sarkar, and **Swarup Bhunia**, “Software Exploitable Hardware Trojan Attacks in Embedded Processor”, *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS)*, 2012. [Special session on hardware security] **[Student Paper Award]**
20. Tina He, Rui Yang, Srihari Rajgopal, Mary Anne Tupta, **Swarup Bhunia**, Mehran Mehregany, and Philip X.-L. Feng, “Robust Silicon Carbide (SiC) Nanoelectromechanical Switches with Long Cycles in Ambient and High Temperature Conditions”, *26th IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, 2013.
21. Abhishek Basak, Vaishnavi Ranganathan, and **Swarup Bhunia**, “A Wearable Ultrasonic Assembly for Point-Of-Care Autonomous Diagnostics of Malignant Growth”, *IEEE EMBS Special Topic Conference on Point-of-Care Healthcare Technologies (PoCHT)*, 2013. **[Student Paper Competition Winner (2nd Place)]**
22. Yu Zheng, Aswin Raghav Krishna, and **Swarup Bhunia**, “ScanPUF: Robust Ultralow Overhead PUF Using Scan Chain”, *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2013.
23. Maryamsadat Hashemian and **Swarup Bhunia**, “Ultralow-Power and Robust Embedded Memory for Bioimplantable Microsystems”, *26th IEEE International Conference on VLSI Design (VLSI-D)*, 2013.
24. Hadi Hajimiri, Prabhat Mishra, and **Swarup Bhunia**, “Dynamic Cache Tuning for Efficient Memory Based Computing in Multicore Architectures”, *26th IEEE International Conference on VLSI Design (VLSI-D)*, 2013.
25. Abhishek Basak, Vaishnavi Ranganathan, Seetharam Narasimhan, and **Swarup Bhunia**, “Implantable Ultrasonic Dual Functional Assembly Detection and Treatment of Anomalous Growth”, *34th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, 2012. **[Student Best Paper Finalist]**
26. Kamran Rahmani, Prabhat Mishra, and **Swarup Bhunia**, “RMBC: Reconfigurable Memory-based Computing for

Performance and Energy Improvement in Multicore Architectures”, 22nd *GLSVLSI Conference*, 2012.

27. [Xinmu Wang](#), [Seetharam Narasimhan](#), and [Swarup Bhunia](#), “SCARE: Side-Channel Analysis based Reverse Engineering for Post-Silicon Validation”, 25th *IEEE International Conference on VLSI Design (VLSI)*, 2012. [Acceptance Rate: 32.7% - 71 out of 218 papers accepted]
28. [Anandaroop Ghosh](#), [Somnath Paul](#), and [Swarup Bhunia](#), “Energy-Efficient Application Mapping in FPGA through Computation in Embedded Memory Blocks”, 25th *IEEE International Conference on VLSI Design (VLSI)*, 2012. [Acceptance Rate: 32.7% - 71 out of 218 papers accepted]
29. [Lei Wang](#), [Somnath Paul](#), and [Swarup Bhunia](#), “Width-Aware Fine-Grained Dynamic Supply Gating: A Design Methodology for Low-Power Datapath and Memory”, 25th *IEEE International Conference on VLSI Design (VLSI)*, 2012. [Acceptance Rate: 32.7% - 71 out of 218 papers accepted] **[Best paper award]**
30. [Rajat Subhra Chakraborty](#), [Seetharam Narasimhan](#) and [Swarup Bhunia](#), “Embedded Software Security through Key-based Control Flow Obfuscation”, *International Conference on Security Aspects in Information Technology, High-Performance Computing and Networking (InfoSecHiComNet)*, 2011. [Acceptance Rate: 12.5% - 14 out of 112 papers accepted]
31. [Abhishek Basak](#), [Seetharam Narasimhan](#), and [Swarup Bhunia](#), “Low Power Implantable Ultrasound Imager for Online Monitoring of Tumor Growth”, 33rd *Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, 2011.
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33. [Xinmu Wang](#), [Seetharam Narasimhan](#), [Somnath Paul](#), and [Swarup Bhunia](#), “NEMTronics: Symbiotic Integration of Nanoelectronic and Nanomechanical Devices for Energy-Efficient Adaptive Computing”, 7th *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, 2011.
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119. **Swarup Bhunia**, Subhasish Majumdar, Ayon Sirkar, and Susmita Sur-kolay, "Topological Routing amidst Polygonal Obstacles", *13th International VLSI Conference (VLSI Design)*, pp. 274-279, 2000.
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Book and Book Chapters:

• Book

1. **Swarup Bhunia**, Steve Majerus, and Mohamad Sawan (Eds.), "Bioimplantable Systems: Design Principles and Applications", Elsevier, MA, USA, to be published in Aug 2014.
2. Somnath Paul and **Swarup Bhunia**, "Computing with Memory for Energy-Efficient Robust Systems", Springer, New York, USA, in progress, to be published in Aug 2013.
3. **Swarup Bhunia** and Saibal Mukhopadhyay (Eds.), "Low-Power Variation-Tolerant Design in Nanometer Silicon", Springer, New York, USA, 1st Edition, ISBN: 978-1-4419-7417-4, November 2010.

• Book Chapters

1. Abhishek Basak and **Swarup Bhunia**, "Implantable Imager for Online Monitoring of Internal Organs", in *Bioimplantable Systems: Design Principles and Applications*", Elsevier, MA, USA, to be published in Aug 2014.
2. Abhishek Basak, Vaishnavi Ranganathan, Seetharam Narasimhan, and **Swarup Bhunia**, "Neural pattern recognition for closed-loop neuro-prosthesis", in "Implantable Bioelectronics - Devices, Materials and Applications", edited by Evgeny Katz, Wiley-VCH, to be published in August 2013.
3. **Swarup Bhunia** and Seetharam Narasimhan, "Hardware Trojan Detection", in "Introduction to Hardware Security and Trust", edited by Mohammad Tehranipoor and Cliff Wang, Springer, New York, USA, September 2011, ISBN: 978-1441980793.
4. **Swarup Bhunia** and Seetharam Narasimhan, "Ultralow Power Implantable Electronics", in "Handbook of Energy-Aware and Green Computing", edited by Sanjay Ranka and Ishfaq Ahmad, Chapman & Hall/CRC Press, Jan 2012, ISBN: 978-1439850404.
5. **Swarup Bhunia** and Kaushik Roy, "Low Power Design Techniques and Test Implications", in "Power-Aware Testing and Test Strategies for Low Power Devices", edited by Patrick Girard, Nicola Nicolici, and Xiaoqing Wen, Springer, New York, USA, 1st Edition, ISBN: 978-1441909275, Aug 2009. [Best-seller in *International Test Conference* 2009].

PROFESSIONAL SERVICES

Editorial Services

- Associate Editor (AE) for ACM Journal on Emerging Technologies in Computing Systems (JETC), Oct 2010 - to date
- Associate Editor, Journal of Low Power Electronics (JOLPE), July 2009 - to date
- Guest Editor, IEEE Design & Test of Computers, special issue on "Trusted System-on-Chip with Untrusted Components", March/April 2013

- Guest Editor, ACM Journal on Emerging Technologies in Computing Systems, special issue on “Implantable Electronics”, June 2012
- Guest Editor, IEEE Design & Test of Computers, special issue on “Post-Silicon Calibration and Repair for Yield and Reliability Improvement”, 2010
- Guest Editor, Journal of Low Power Electronics (JOLPE), special issue on low power track paper in International Conference of VLSI Design, 2010

Program Committee Services (Organizing Committee)

- Program Chair, IEEE/ACM International Symposium of Nanoscale Architectures (NANOARCH), 2013
- Publicity Chair, IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2013
- Publicity Chair, International Conference on Security, Privacy and Applied Cryptography Engineering (SPACE), 2012
- Program Chair, International Mixed-Signals, Sensors, and Systems Test Workshop (IMS3TW), 2011
- Publication Chair, 11th IEEE International On-Line Testing Symposium (IOLTS), 2005

Program Committee Services (Technical Program Committee)

- Track Chair for Track T6-Devices, Circuits and Systems for Emerging Technologies, 21st IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 2013.
- Technical Program Committee Member, 3rd International Conference on Security, Privacy, and Applied Cryptography Engineering (SPACE), 2013
- Technical Program Committee Member, 5th IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2013
- Technical Program Committee Member, 26th International Conference on VLSI Design (VLSI Design), 2013
- Program Committee Member, 14th Workshop on Cryptographic Hardware and Embedded Systems (CHES), 2012
- Technical Program Committee Member, 18th IEEE International Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW), 2012
- Technical Program Committee Member, 4th IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2012
- Technical Program Committee Member, 25th International Conference on VLSI Design (VLSI Design), 2012
- Program Committee Member, 13th Workshop on Cryptographic Hardware and Embedded Systems (CHES), 2011
- Technical Program Committee Member, 7th IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), 2011
- Program Committee Member, International Conference on Security Aspects in Information Technology, High-Performance Computing and Networking (InfoSecHiComNet), 2011
- Technical Program Committee Member, Design Automation and Test in Europe (DATE), 2011
- Technical Program Committee Member, IEEE International Symposium on VLSI (ISVLSI), 2011
- Technical Program Committee Member, 20th IEEE Asian Test Symposium (ATS), 2011
- Technical Program Committee Track Chair (Low Power Track), International Conference on VLSI Design (VLSI Design), 2011
- Technical Program Committee Track Chair (low power track), International Conference on VLSI Design (VLSI Design), 2010
- Member of Technical Program Committee, Design Automation and Test in Europe (DATE), 2006-2010
- Member of Technical Program Committee, IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2007-2010
- Member of Technical Program Committee of IEEE International Conference on VLSI (ISVLSI), 2008-2010
- Member of Technical Program Committee, IEEE/ACM Nanoscale Architecture Symposium (NANOARCH), 2007-2010
- Member of Program Committee, IEEE Hardware Oriented Security and Test (HOST) Symposium, 2008-2010

- Member of program committee, Test Technology Educational Program (TTEP) by IEEE Computer Society, 2006-2009
- Member of Technical Program Committee of IFIP/IEEE International Conference on VLSI (VLSI-SoC), 2008

Other Professional Services

- Organizer of a Panel in the 9th IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), 2013
- Technical Program Session Chair, IEEE Symposium on Hardware Oriented Security and Trust (HOST), 2013
- Technical Program Session Chair, 34th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), 2012
- Organizer & Moderator of Hot Topic Special Session in IEEE VLSI Test Symposium (VTS), 2010
- Technical Program Session Chair, IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), 2010
- Technical Program Session Chair, IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2010
- Created an Internet Group on “Hardware Security” in social networking website Facebook (currently with ~160 members from around the world), 2010
- Created a Wiki page on Hardware Obfuscation in the area of hardware security, 2010
- Created a Wiki page on Computing with Memory in the area of reconfigurable computing with memory, 2010
- Faculty member and advisor for (HKN) Eta Kappa Nu (Electrical Engineering honor society), since April, 2010
- Technical Program Session Chair, International conference on VLSI Design (VLSI Design), 2010
- Contribution of presentation materials on “[Low-Power and Robust Logic Design](#)” to Synopsys University Program, 2008
- Technical Program Session Chair, IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), 2008
- Technical Program Session Chair, International Symposium on Low Power Electronics and Design (ISLPED), 2007
- Technical Program Session Moderator, IEEE International Conference on Computer Aided Design (ICCAD), 2007
- **Reviewer:** *IEEE Trans. VLSI Systems (TVLSI)*, *IEEE Trans. on CAD (TCAD)*, *IEEE Trans. on Computers (TComp)*, *IEEE Trans. on Circuits and Systems (TCAS)*, *Journal of Electronic Testing: Theory and Applications (JETTA)*, *ACM Trans. on Design Automation of Electronic System (TODAES)*, *IEEE Design & Test of Computers*, *ACM Journal of Emerging Tech. and Comp. (JETC)*, *IEEE Embedded Systems Letter (ESL)*, *IEEE Transactions on Information Forensics and Security (TIFS)*, *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, *IEEE Electron Device Letters (EDL)*, *IEEE Transactions on Biomedical Circuits and Systems (TBioCAS)*, *Journal of Neural Engineering (JNE)*

UNIVERSITY/SCHOOL/DEPARTMENT SERVICE:

- EECS Chair Search Committee Member, Spring 2013
- Academic Representative for Computer Engineering, 2011-2013
- Senior Project Advising: Spring 2013
 - Two Groups: Patrick Landis & Schuyler Thomson | Timothy March and Linneker Carvajal
- Research showcase judge, April 12, 2013
- Participation in ABET 2012 program committee representing Computer Engineering program
- Help with Distinguished speaker series seminar:
 - Dr. John Carter, IBM Austin Research Lab, Manager, Power-Aware Systems, April 21, 2011
 - Dr. Dave Ferucci, IBM Fellow, the Chief Scientist for Watson machine, Oct 4, 2011

- Dr. Vivek De, Intel Fellow, Director of Intel Circuit Labs, Oct 19, 2012
- Oral qualifier exam committee, Srihari Rajgopal, Oct 2012
- Choices Fair CE Representative, Oct 2012
- Freshman advisor (SGAES freshman course) Fall 2012
- Academic Representative for Computer Engineering, 2011-2012
- Academic Representative for Computer Engineering, 2012-2013
- ABET committee representing CE program, 2011-2012
- University *UUF Academic Standing Committee* member, 2009-2010
- Case School of Engineering (CSE) *Research Committee* member, 2009-2010
- EECS *Curriculum and Accreditation Committee* Member, 2005, 2007-2009
- Departmental Open house, 2009
- Sophomore/Junior CE Undergraduate Advisor, 2006-2010
- Research Showcase Judge, 2007-2010
- Computer Engineering Program Representative, Fall 2007
- Organizer of Departmental Town-Hall Meeting, 2006
- **PhD Thesis Committee Member:** Jen-Chieh Ou (EECS, CWRU), Jung Hwan Choi (ECE, Purdue University), Hyun Kim (EECS, CWRU), Huthaifa Al-Omari (EECS, CWRU), Te-Hao Lee (EECS, CWRU), Steve Majerus (EECS, CWRU), Zheng Liu (CS, CWRU), Steve Majerus (EE, CWRU) 2012, Kanokwan (Nok) Limnusun (EE, CWRU) 2012, Chia-Wei Soong (EE, CWRU) 2013, Bobby Lu (EE, CWRU) 2013, Steve Majerus (EE, CWRU) 2013
- **MS Thesis committee member:** Moiz Neemuchwala (EECS, CWRU), Sivasubramaniam Krishnamurthy (EECS, CWRU), Pranay Nigam (EECS, CWRU), Manjulatha Kamalraj (EECS, CWRU), David Young (EECS, CWRU), Prasanna V. Govindarajan (EECS, CWRU), Shruthi Rnganathan (EECS, CWRU), Zemeng Li (EECS, CWRU), Ying Ying Wang (EECS, CWRU), Ming-Hsuan Hsu (EECS, CWRU), Nitin Reddy (EECS, CWRU), David Tian (EECS, CWRU), Patrick Rawlinson (EECS, CWRU), Prapan Shewinvanakitkul (EECS, CWRU), Tyler Goeringer (CS, CWRU) 2013

PRESENTATIONS / SEMINAR

[Presentations marked in blue are made after joining Case. Underlined presenter is a Case student supervised by Dr. Bhunia. All conference presentations listed here are made by either Dr. Bhunia or his student advisee.]

Invited presentations:

1. Presentation to Intel Corporation, Portland, Microprocessor Research Lab, on memory-centric scalable co-processor (via Telecon), April 5, 2013
2. Presentation at University of Florida, Dept. of CISE, on Hardware Security, March 15, 2013
3. Presentation at Texas Instruments, Dallas (Microcontroller group) on Energy-Efficient Computing, March 13, 2013
4. Presentation at Lockheed Martin, Akron, OH as an guest speaker in the Engineer's Week celebration, on security of electronics, February 19, 2013
5. Presentation to Intel Research, Portland, OR, USA on In-Memory Acceleration, Nov 20, 2012 (via Telecon)
6. Presentation in Design and Test Summer School, Oct 25-26, Puebla, Mexico, organized by National Institute for Astrophysics, Optics, and Electronics, (INAOE), Mexico
7. Presentation in Qualcomm, Inc. San Diego on Adaptive Computing for Low Power and Variation Tolerance, Aug 2012
8. Presentation at IBM TJ Watson Research Lab (New York, USA) on nanocomputing architecture, June 2012
9. Presentation at Indian Institute of Technology (IIT), Kharagpur on nano-computing, Jan 2012
10. Presentation at Korea University, Seoul, Korea, on low-power and robust nanoscale architecture, Aug 2011
11. Presentation at *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug 2011 in

special session on self-healing circuits

12. Presentation in ARO Special Workshop on Hardware Assurance in Washington DC, Monday, April 11, 2011
13. Presentation in IBM Austin Research Lab (ARL), Austin, TX, Monday, Nov 1, 2010
14. Presentation at Intel Corporation workshop on external academic research, Portland, OR, USA, Sept 27, 2010
15. Panelist in *IEEE International Symposium on Nanoscale Architecture (NANOARCH)*, Panel on “CAD for Nanoelectronic Circuit and Architecture - Are we there yet” with Alan Mishchenko (UC Berkeley), Krill Minkovich (UCLA), Kaustav Banerjee (UCSB), Mark Riedel (UMN), Bao Liu (UTexas, San Antonio), Moderator: Garrett S. Rose (NYU-Poly), 2010
16. Panelist in *IEEE Hardware Oriented Security and Trust (HOST)*, Panel on “Challenges in Hardware Trojan Modeling and Detection”, with Miron Abramovici (Tiger’s Lair), Mohammad Tehranipoor (UConn), CJ Clark (Intellitech), Eric Sivertson (Quantumtrace), Moderator: James Plusquellic (UNM), 2010
17. Presentation on “Adaptive Computing” at Intel Circuit Research Lab (CRL), Portland, OR, USA, Aug 1, 2010.
18. Presentation at “*Apprentice - VTS Edition: Season 3*”, Organizer/Moderator: K. S. Kim – Samsung, *IEEE VLSI Test Symposium (VTS)*, 2010
19. Presentation at *The Asia Symposium on Quality Electronic Design (ASQED)* on “Digital Signal Processing in Bio-implantable Systems: Design Challenges and Emerging Solutions”, 2010
20. Presentation at *IEEE International High Level Design Validation and Test Workshop (HLDVT)* on “Hardware Trojan: Threats and Emerging Solutions”, 2009
21. Presentation at *IEEE International Symposium on Nanoscale Architecture (NANOARCH)* on “Computing with Nanoscale Memory: Model and Architecture”, 2009
22. Lecture series presentation at *International Test Conference (ITC)* on “Power Dissipation, Variations and Nanoscale CMOS Design: Test Challenges and Self Calibration/Self Repair Solutions”, Oct 2007
23. Presentation at *Intel Corporation*, Bangalore, India, Jan, 2010
24. Presentation at *Cryptography Research Institute (CRI)*, San Francisco, CA, USA, 2009
25. Presentation to Circuit Research Lab, *Intel Corporation*, Portland, OR, USA, Feb 2008
26. Presentation on efficient speed binning, LSI Technologies, Oct, 2007.
27. Presentation to Circuit Research Lab, *Intel Corporation*, Portland, OR, USA, Nov, 2007
28. Presentation at *Indian Institute of Technology (IIT)*, Department of Computer Sc., Kharagpur, India, 2006
29. IEEE series presentation at *Jadavpur University*, Dept of Electronics & Telecommunications Eng, Kolkata, India, 2006

Tutorials (Full Day / Half-Day):

1. Srivaths Ravi, Anand Rangunathan, Eric Peeters, and **Swarup Bhunia**, “Designing Secure SoCs”, upcoming in 26th *IEEE International Conference on VLSI Design (VLSI)*, 2013. Organizer: Srivaths Ravi, Texas Instruments. [**Full-Day Tutorial**]
2. Susmita Sur-Kolay and **Swarup Bhunia**, “Intellectual Property Protection and Security in System on a Chip”, in 25th *IEEE International Conference on VLSI Design (VLSI)*, 2012. Organizer: Susmita Sur-Kolay, Indian Statistical Institute. [**Full-Day Tutorial**]
3. Rahul Rao, Saibal Mukhopadhyay, **Swarup Bhunia**, and Praveen Elakkumanan, “*Parameter Variations and Low-Power Design: Test Issues and On-chip Calibration/Repair Solutions*”, in *International Test Conference (ITC)*, 2010. Organizer: Rahul Rao, IBM Research. [**Full-Day Tutorial**]
4. Rahul Rao, Saibal Mukhopadhyay, **Swarup Bhunia**, and Praveen Elakkumanan, “*Parameter Variations and Low-Power Design: Test Issues and On-chip Calibration/Repair Solutions*”, in *VLSI Test Symposium (VTS)*, 2010. Organizer: Rahul Rao, IBM Research. [**Full-Day Tutorial**]
5. Rahul Rao, Praveen Elakkumanan, Saibal Mukhopadhyay and **Swarup Bhunia**, "Parametric Failures and Self-Calibration/Self-Repair Solutions", in *International Test Conference (ITC)*, 2009. Organizer: Saibal Mukhopadhyay, Georgia Tech. [**Full-Day Tutorial**]
6. **Swarup Bhunia**, Kanak B. Agarwal and Kaushik Roy, "Low Power Design under Parameter Variations", in *Design Automation and Test in Europe (DATE) Conference*, 2009. Organizer: Swarup Bhunia, Case Western

Reserve U. [**Half-Day Tutorial**]

7. Saibal Mukhopadhyay, Rahul Rao, Praveen Elakkumanan, and **Swarup Bhunia**, "Parametric Failures and Self-Calibration/Self-Repair Solutions in Nanometer Technologies", in *IEEE International On-Line Test Symposium (IOLTS)*, 2009. Organizer: Saibal Mukhopadhyay, Georgia Tech. [**Full-Day Tutorial**]
8. **Swarup Bhunia**, "Variation-Tolerant Low-Power Logic Circuit", in *International Symposium on Quality Electronic Design (ISQED)*, 2009. Organizer: Rajiv Joshi, IBM Research. [**Embedded Tutorial**]
9. **Swarup Bhunia** and Kaushik Roy, "Low Power Design under Parameter Variations", in *IEEE International SOC Conference (SOCC)*, 2008. Organizer: Swarup Bhunia, Case Western Reserve U. [**Half-Day Tutorial**]
10. Kaushik Roy and **Swarup Bhunia**, "Low Power Design under Parameter Variations", in *International Symposium on Low Power Electronics and Design (ISLPED)*, 2008. Organizer: Swarup Bhunia, Case Western Reserve U. [**Embedded Tutorial**]
11. **Swarup Bhunia** and Kaushik Roy, "Process Variations and Process-Tolerant Design", in *International Conference on VLSI Design*, 2007. Organizer: Swarup Bhunia, Case Western Reserve U. [**Embedded Tutorial**]

Conference Presentations

1. Xinmu Wang, Wen Yueh, Debapriya Basu Roy, Yu Zheng, Seetharam Narasimhan, Saibal Mukhopadhyay, Debdeep Mukhopadhyay, and **Swarup Bhunia**, "Role of Power Grid in Side Channel Attack and Power-Grid-Aware Secure Design", in *Design Automation Conference (DAC)*, 2013.
2. Yu Zheng, Aswin Raghav Krishna, and **Swarup Bhunia**, "ScanPUF: Robust Ultralow Overhead PUF Using Scan Chain", in *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2013.
3. Maryamsadat Hashemian and **Swarup Bhunia**, "Ultralow-Power and Robust Embedded Memory for Bioimplantable Microsystems", in *26th IEEE International Conference on VLSI Design (VLSI-D)*, 2013.
4. Xinmu Wang, Seetharam Narasimhan, and **Swarup Bhunia**, "SCARE: Side-Channel Analysis based Reverse Engineering for Post-Silicon Validation", *25th IEEE International Conference on VLSI Design (VLSI)*, 2012.
5. Anandaroop Ghosh, Somnath Paul, and **Swarup Bhunia**, "Energy-Efficient Application Mapping in FPGA through Computation in Embedded Memory Blocks", *25th IEEE International Conference on VLSI Design (VLSI)*, 2012.
6. Lei Wang, Somnath Paul, and **Swarup Bhunia**, "Width-Aware Fine-Grained Dynamic Supply Gating: A Design Methodology for Low-Power Datapath and Memory", *25th IEEE International Conference on VLSI Design (VLSI)*, 2012.
7. Fall 2011 EECS 500 Departmental Seminar on Computer Engineering Research Program, Sept 13, 2011
8. Abhishek Basak, Seetharam Narasimhan, and **Swarup Bhunia**, "Low Power Implantable Ultrasound Imager for Online Monitoring of Tumor Growth", in *33rd Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, 2011.
9. Aswin Raghav Krishna, Seetharam Narasimhan, Xinmu Wang, and **Swarup Bhunia**, "MECCA: A Robust Low-Overhead PUF using Embedded Memory Array", in *Workshop on Cryptographic Hardware and Embedded Systems (CHES)*, 2011.
10. Xinmu Wang, Seetharam Narasimhan, Somnath Paul, and **Swarup Bhunia**, "NEMTronics: Symbiotic Integration of Nanoelectronic and Nanomechanical Devices for Energy-Efficient Adaptive Computing", *7th IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, 2011.
11. Abhishek Basak, Seetharam Narasimhan, and **Swarup Bhunia**, "KiMS: Kids' Health Monitoring System at Day-Care Centers using Wearable Sensors and Vocabulary-based Acoustic Signal Processing", *13th IEEE International Conference on e-Health Networking, Application & Services (Healthcom)*, 2011.
12. Seetharam Narasimhan, Xinmu Wang, Dongdong Du, Rajat Subhra Chakraborty, and **Swarup Bhunia**, "TeSR: A Robust Temporal Self-Referencing Approach for Hardware Trojan Detection", *4th IEEE International Symposium on Hardware-Oriented Security and Trust (HOST)*, 2011.
13. Dongdong Du, Seetharam Narasimhan, Rajat Subhra Chakraborty and **Swarup Bhunia**, "Self-Referencing: A Scalable Side-Channel Approach for Hardware Trojan Detection", *Workshop on Cryptographic Hardware and Embedded Systems (CHES)*, 2010.
14. Somnath Paul and **Swarup Bhunia**, "VAIL: Variation-Aware Issue Logic and Performance Binning for

- Processor Yield and Profit Improvement”, *International Symposium on Low Power Electronics and Design (ISLPED)*, 2010.
15. Dongdong Du, Seetharam Narasimhan, Rajat Subhra Chakraborty, Chris Papachristou, Somnath Paul, and **Swarup Bhunia**, “Multiple-Parameter Side-Channel Analysis: A Non-invasive Hardware Trojan Detection Approach”, *IEEE Symposium on Hardware Oriented Security and Trust (HOST)*, 2010.
 16. **Rajat Subhra Chakraborty** and **Swarup Bhunia**, “RTL Hardware IP Protection Using Key-Based Control and Data Flow Obfuscation”, *23rd International Conference on VLSI Design*, 2010.
 17. **Somnath Paul**, Saibal Mukhopadhyay and **Swarup Bhunia**, "A Variation-Aware Preferential Design Approach for Memory Based Reconfigurable Computing," *IEEE International Conference on Computer Aided Design (ICCAD)*, 2009.
 18. **Rajat Subhra Chakraborty** and **Swarup Bhunia**, "Security through Obscurity: An Approach for Protecting Register Transfer Level Hardware IP," *IEEE Hardware Oriented Security and Trust (HOST) Workshop*, 2009. [Poster Presentation]
 19. **Rajat Subhra Chakraborty** and **Swarup Bhunia**, "Security against Hardware Trojan through a Novel Application of Design Obfuscation," *IEEE International Conference on Computer Aided Design (ICCAD)*, 2009.
 20. Rajat Subhra Chakraborty, Francis Wolff, Somnath Paul, Christos Papachristou and **Swarup Bhunia**, "MERO: A Statistical Approach for Hardware Trojan Detection," *Workshop on Cryptographic Hardware and Embedded Systems (CHES)*, 2009.
 21. **Seetharam Narasimhan**, Hillel J. Chiel and **Swarup Bhunia**, “A Preferential Design Approach for Energy-Efficient and Robust Implantable Neural Signal Processing”, *IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, 2009.
 22. **Rajat Subhra Chakraborty** and **Swarup Bhunia**, “Hardware Protection Through Netlist-Level Obfuscation”, under review in *IEEE International Conference on Computer Aided Design (ICCAD)*, 2008.
 23. **Somnath Paul**, Saibal Mukhopadhyay, and **Swarup Bhunia**, “Hybrid CMOS-STTRAM FPGA Design Optimization for Low Power and High Integration Density”, *IEEE International Conference on Computer Aided Design (ICCAD)*, 2008.
 24. **Seetharam Narasimhan**, Miranda Cullins, Hillel Chiel, and **Swarup Bhunia**, “Wavelet-Based Neural Pattern Analyzer for Behaviorally Significant Burst Pattern Recognition”, *IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, 2008. [Poster Presentation]
 25. **Rajat Subhra Chakraborty**, Somnath Paul, and **Swarup Bhunia**, “On-Demand Transparency for Improving Hardware Trojan Detectability”, *IEEE Hardware Oriented Security and Trust (HOST) Workshop*, 2008.
 26. **Seetharam Narasimhan**, Somnath Paul, and **Swarup Bhunia**, “Collective Computing Based on Swarm Intelligence”, *Design Automation Conference (DAC)*, 2008 [as a WACI (Wild and Crazy Ideas) paper].
 27. **Somnath Paul** and **Swarup Bhunia**, “Reconfigurable Computing Using Content Addressable Memory for Improved Performance and Resource Usage”, *Design Automation Conference (DAC)*, 2008.
 28. **Matthew Holtz**, **Seetharam Narasimhan**, and **Swarup Bhunia**, “On-die CMOS Voltage Droop Detection and Dynamic Compensation”, *Great Lakes Symposium on VLSI (GLSVLSI)*, 2008.
 29. **Rajat Subhra Chakraborty** and **Swarup Bhunia**, “Micropipeline-Based Asynchronous Design Methodology for Robust System Design Using Nanoscale Crossbar”, *IEEE International Symposium on Quality Electronic Design (ISQED)*, 2008.
 30. **Seetharam Narasimhan**, Miranda Cullins, Hillel Chiel, and **Swarup Bhunia**, “Wavelet Based Neural Pattern Analyzer in Aplysia for Closed-Loop Neuroprosthesis”, *Research ShowCase*, 2008. [Poster Presentation]
 31. **Yu Zhou**, **Somnath Paul**, and **Swarup Bhunia**, “Towards Uniform Temperature Distribution in SOI Circuits Using Carbon Nanotube Based Thermal Interconnect”, *IEEE International Symposium on Quality Electronic Design (ISQED)*, 2008.
 32. **Lawrence Leinweber** and **Swarup Bhunia**, “Fine-Grained Supply Gating Through Hypergraph Partitioning and Shannon Decomposition for Active Power Reduction”, *Design Automation and Test in Europe (DATE)*, 2008.
 33. **Yu Zhou**, **Somnath Paul** and **Swarup Bhunia**, “Harvesting Wasted Heat in a Microprocessor Using Thermo-Electric Generators: Modeling, Analysis and Measurement”, *Design Automation and Test in Europe (DATE)*, 2008.
 34. **Rajat Subhra Chakraborty**, **Somnath Paul**, and **Swarup Bhunia**, "Analysis and Robust Design of Diode-

- Resistor Based Nanoscale Crossbar PLA Circuits", *International Conference on VLSI Design*, 2008.
35. [Somnath Paul](#) and **Swarup Bhunia**, "MBCAR: A Scalable Memory Based Reconfigurable Computing Framework for Nanoscale Devices", *Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2008.
 36. [Seetharam Narasimhan](#), Yu Zhou, Hillel J. Chiel, and **Swarup Bhunia**, "Low-Power VLSI Architecture for Neural Data Compression Using Vocabulary-based Approach", *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2007.
 37. [Somnath Paul](#) and **Swarup Bhunia**, "Memory Based Computation Using Embedded Cache for Processor Yield and Reliability Improvement", *International Conference on Computer Design (ICCD)*, 2007.
 38. [Somnath Paul](#), Siva Krishnamurthy, Hamid Mahmoodi, and **Swarup Bhunia**, "Low-Overhead Design Technique for Calibration of Maximum Frequency at Multiple Operating Points", *IEEE International Conference on Computer Aided Design (ICCAD)*, 2007.
 39. [Yu Zhou](#), Shijo Thekkel, and **Swarup Bhunia**, "Low power FPGA Design Using Hybrid CMOS-NEMS Approach", *International Symposium on Low Power Electronics and Design (ISLPED)*, 2007.
 40. [Seetharam Narasimhan](#), Massood Tabib-Azar, Hillel J. Chiel, and **Swarup Bhunia**, "Neural Data Compression with Wavelet Transform: A Vocabulary Based Approach", *IEEE EMBS Conference on Neural Engineering*, 2007.
 41. Somnath Paul, [Rajat Subhra Chakraborty](#), and **Swarup Bhunia**, "VIm-Scan: A Low Overhead Scan Design Approach for Protection of Secret Key in Scan-Based Secure Chips", *IEEE VLSI Test Symposium (VTS)*, 2007.
 42. Siva Krishnamurthy, [Somnath Paul](#), and **Swarup Bhunia**, "Adaptation to Temperature-Induced Delay Variations in Logic Circuits Using Low-Overhead Online Delay Calibration", *IEEE International Symposium on Quality Electronic Design (ISQED)*, 2007.
 43. **Swarup Bhunia**, Massood Tabib Azar, and Daniel Saab, "Ultralow-Power Adaptive System Architecture Using Complementary Nano-Electromechanical Carbon Nanotube Switches," *NANOARCH*, Boston, MA, 2006.
 44. Nilanjan Banerjee, **Swarup Bhunia**, Hamid Mahmoodi, and Kaushik Roy, "Low Power Synthesis of Dynamic Logic Circuits Using Fine-Grained Clock Gating", *Design Automation and Test in Europe (DATE)*, 2006.
 45. Arijit Raychowdhury, Bipul Chandra Paul, **Swarup Bhunia**, Kaushik Roy, "Ultralow power computing with sub-threshold leakage: a comparative study of bulk and SOI technologies", *Design and Test in Europe (DATE)*, 2006.
 46. **Swarup Bhunia**, Hamid Mahmoodi, Nilanjan Banerjee, Qikai Chen, and Kaushik Roy, "A Novel Synthesis Approach for Active Leakage Power Reduction Using Supply Gating", *Design Automation Conference (DAC)*, 2005.
 47. Animesh Datta, **Swarup Bhunia**, Saibal Mukhopadhyay, Kaushik Roy, "A Statistical Approach to Area-Constrained Yield Enhancement for Pipelined Circuits under Parameter Variations", *Asian Test Symposium (ATS)*, 2005.
 48. Swaroop Ghosh, **Swarup Bhunia**, Kaushik Roy, "Shannon Expansion Based Supply-Gated Logic for Improved Power and Testability", *Asian Test Symposium (ATS)*, 2005.
 49. Lih-yih Chiou, **Swarup Bhunia**, and Kaushik Roy, "Synthesis of Application Specific Multi-Mode Systems", *Design automation and Test in Europe (DATE)*, 2003.
 50. **Swarup Bhunia** and Kaushik Roy, "Dynamic Supply Current Testing of Analog Circuits Using Wavelet Transform", *VLSI Test Symposium (VTS)*, 2002.
 51. **Swarup Bhunia** and Kaushik Roy, "A Novel Wavelet Transform Based Transient Current Analysis for Fault Detection and Localization", *Design Automation Conference (DAC)*, 2002.
 52. **Swarup Bhunia**, Subhasish Majumdar, Ayon Sirkar, and Susmita Sur-kolay, "Topological Routing amidst Polygonal Obstacles", *13th International VLSI Conference (VLSI Design)*, India, 2000.
 53. **Swarup Bhunia**, Soumya Ghosh, Pramod Kumar, Partha Das, and Jayanta Mukherjee, "Design, Simulation and Synthesis of an ASIC for Fractal Image Coding", *12th International VLSI Conference (VLSI Design)*, India, 1999.

STUDENT ACCOMPLISHMENTS:

Awards:

- High School student Tatini Mal-Sarkar working in Nanoscape lab for 4 years is selected as **Rabi Scholar** in Columbia University, April 2013
- **Best student paper award** in 8th IEEE International Conference on Nano/Micro Engineered and Molecular Systems (NEMS) for collaborative work with Prof. Philip Feng and Prof. Mehran Mehregany.
- High School student Tatini Mal-Sarkar wins the **Student Paper Award** (Sponsored by Intel Corporation) in 25th IEEE IEEE International Symposium on Defect and Fault Tolerance in VLSI & Nanotechnology Systems (DFTS), 2012.
- Graduate student Abhishek Basak and Vaishnavi Ranganathan's **wins the Student Paper Competition** (second place) in IEEE EMBS Special Topic Conference on Point-of-Care Healthcare Technologies (PoCHT), 2013
- Graduate student Abhishek Basak and Vaishnavi Ranganathan's paper is selected Student Paper Competition (SPC) Finalist in IEEE EMBS Special Topic Conference on Point-of-Care Healthcare Technologies (PoCHT), 2013
- Graduate student Abhishek Basak is selected Student Paper Competition (SPC) Finalist for 34th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), 2012
- Graduate student Somnath Paul receives the **EDAA Outstanding Dissertation Award** from the European Design Automation Association, 2012
- Graduate student Somnath Paul earned **Ruth Barber Moon award**, Case Western Reserve University from the Case School of Graduate Studies for excellence in academic promise and leadership quality, 2011
- Graduate students Xinmu Wang, Aswin Krishna, and Seetharam Narasimhan **won the Third Prize** in the NYU-Poly CSAW Hardware Trojan Design Challenge [7th Annual CSAW Challenge], 2010
- Graduate student Seetharam Narasimhan selected as **Open Finalist** in the IEEE Engineering in Medicine and Biology Society (EMBS) Student Paper Competition, 2009
- Graduate student Rajat Subhra Chakraborty earned **Ruth Barber Moon award**, Case Western Reserve University from the Case School of Graduate Studies for excellence in academic promise and leadership quality, 2009
- Graduate student Seetharam Narasimhan earned **Ruth Barber Moon award**, Case Western Reserve University from the Case School of Graduate Studies for excellence in academic promise and leadership quality, 2008

Other Achievements:

- Senior project by team by Patrick Landis and Schuyler Thomson is awarded best senior project in the department of EECS, Spring 2013
- Nanoscape Team (Xinmu Wang, Tatini Mal-Sarkar, Patrick Feeley, and Timothy March) is selected Finalist in [Embedded Systems Challenge \(ESC\)](#) in NYU-Poly Cyber Security Awareness Week, 2012
- Graduate student Vaishnavi Ranganathan and Anandaroop Ghosh receives the Young student fellowship (YSSP) in Design Automation Conference (DAC), 2012
- Graduate student Abhishek Basak gets nominated for the HHMI International Student Research Fellowship by Case Western Reserve University, Nov 2011
- Nanoscape Team (Xinmu Wang, Seetharam Narasimhan, Tatini Mal-Sarkar, and Aswin Krishna) is selected Finalist in [Embedded Systems Challenge \(ESC\)](#) in NYU-Poly Cyber Security Awareness Week, 2011
- Graduate student Somnath Paul's thesis topic has been selected as semi-finalist in *ACM Student Research Competition* at 47th Design Automation Conference (DAC) 2010
- Graduate student Seetharam Narasimhan's Phd Topic has been selected in Design Automation Conference (DAC) PhD forum, 2010
- Graduate student Xinmu Wang receives the Young student fellowship (YSSP) in Design Automation Conference (DAC), 2010
- High-school student Tatini Mal-Sarkar published white paper on "Collaborative Trust: A Novel Paradigm of Trusted Mobile Computing", in online archive and trusthub.org <http://arxiv.org/ftp/arxiv/papers/1010/1010.2447.pdf>, and in trust-hub, Oct 2010
- Graduate student Rajat Subhra Chakraborty's Ph.D. thesis abstract has been selected for semi-final round of the *TTTC E. J. McCluskey Best Doctoral Thesis Award* contest, held at the IEEE VLSI Test Symposium (VTS), 2010

- Graduate students Seetharam Narasimhan, Dongdong Du, Rajat Chakraborty, Xinmu Wang selected Finalist of the NYU-Poly CSAW Embedded Systems Challenge [6th Annual CSAW Challenge], 2009
- Graduate student Rajat Subhra Chakraborty's Phd Topic has been selected in Design Automation Conference (DAC) PhD forum, 2009
- Graduate student Rajat Subhra Chakraborty receives the Young student fellowship (YSSP) in Design Automation Conference (DAC), 2008

GRADUATED STUDENTS:

PHD:

1. Seetharam Narasimhan (PhD with thesis, April 2012), currently at Intel Corporation, security group, Portland, Oregon, USA
2. Rajat Subhra Chakraborty (PhD with thesis, June 2010), currently a tenure-track assistant professor at Indian Institute of Technology (IIT), Kharagpur, India
3. Somnath Paul (PhD with thesis, July 2011), currently at Intel Research Lab, Portland, Oregon, USA.
4. Xinmu Wang (PhD with thesis, August 2013, upcoming), at Qualcomm Inc., San Diego, CA, USA.

MS:

1. Vaishnavi Ranganathan (MS with Thesis, June 2013)
2. MaryamSadat Hashemian (MS with Thesis, June 2013)
3. Anandaroop Ghosh (MS with Thesis, March 2013), currently at Intel Corporation, Portland, OR, USA
4. Lei Wang (MS with Thesis, 2012)
5. E-Jen Lien (MS with Thesis, 2012)
6. Keerthi Kunaparaju (MS with thesis, 2011), currently at Intel Corporation, Phoenix, AZ, USA
7. Yu Zhou (MS with thesis, 2007), currently at Marvel Semiconductor, San Jose, USA
8. Dongdong Du (MS with thesis, 2010), currently at Hyland Software, Westlake, OH, USA
9. David Stalter (MS with thesis, 2010), currently at Rockwell Automation, Cleveland, OH, USA
10. Lawrence Leinweber (MS with thesis, 2007), currently at Andeen-Hagerling Inc., Solon, Ohio
11. Matthew Holtz (MS with project, 2007), currently at Keithley Instruments Inc., Cleveland, OH, USA

COLLABORATORS

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TEACHING

Fall 2005: EECS 600 – Nanometer VLSI Design (Graduate)
 Spring 2006: EECS 314 – Computer Architecture (Undergraduate)
 Fall 2006: EECS 600 – Nanometer VLSI Design (Graduate)
 Spring 2007: EECS 314 – Computer Architecture (Undergraduate)
 Fall 2007: EECS 495 – Nanometer VLSI Design (Graduate)
 Spring 2008: EECS 314 – Computer Architecture (Undergraduate)
 Fall 2008: EECS 495 – Nanometer VLSI Design (Graduate)
 Fall 2008: EECS 301 – Digital Logic Laboratory (Undergraduate)
 Spring 2009: EECS 314 – Computer Architecture (Undergraduate)
 Fall 2009: EECS 495 – Nanometer VLSI Design (Graduate)
 Fall 2009: EECS 301 – Digital Logic Laboratory (Undergraduate)
 Spring 2010: EECS 314 – Computer Architecture (Undergraduate)
 Fall 2010: EECS 495 – Nanometer VLSI Design (Graduate)
 Fall 2010: EECS 301 – Digital Logic Laboratory (Undergraduate)

Spring 2011: EECS 314 – Computer Architecture (Undergraduate)
Spring 2011: EECS 397 – Hardware Security (New Undergraduate Course Introduced in Spring 2011)
Fall 2011: EECS 495 – Nanometer VLSI Design (Graduate)
Fall 2011: EECS 301 – Digital Logic Laboratory (Undergraduate)
Spring 2012: EECS 314 – Computer Architecture (Undergraduate)
Spring 2012: EECS 397 – Hardware Security (Undergraduate)
Fall 2012: FSNA 137 – Sages First Seminar Course “Volts, Amps, Bits, Bytes” (New Undergraduate Course introduced in Fall 2012)
Spring 2013: EECS 314 – Computer Architecture (Undergraduate)
Fall 2013: FSNA 137 – Sages First Seminar Course “Volts, Amps, Bits, Bytes” (Undergraduate)